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MULTIPLE ERASE BLOCK TAGGING IN A FLASH MEMORY DEVICE
Atty Docket No. 400.240US01 Serial No.: 10/363,179

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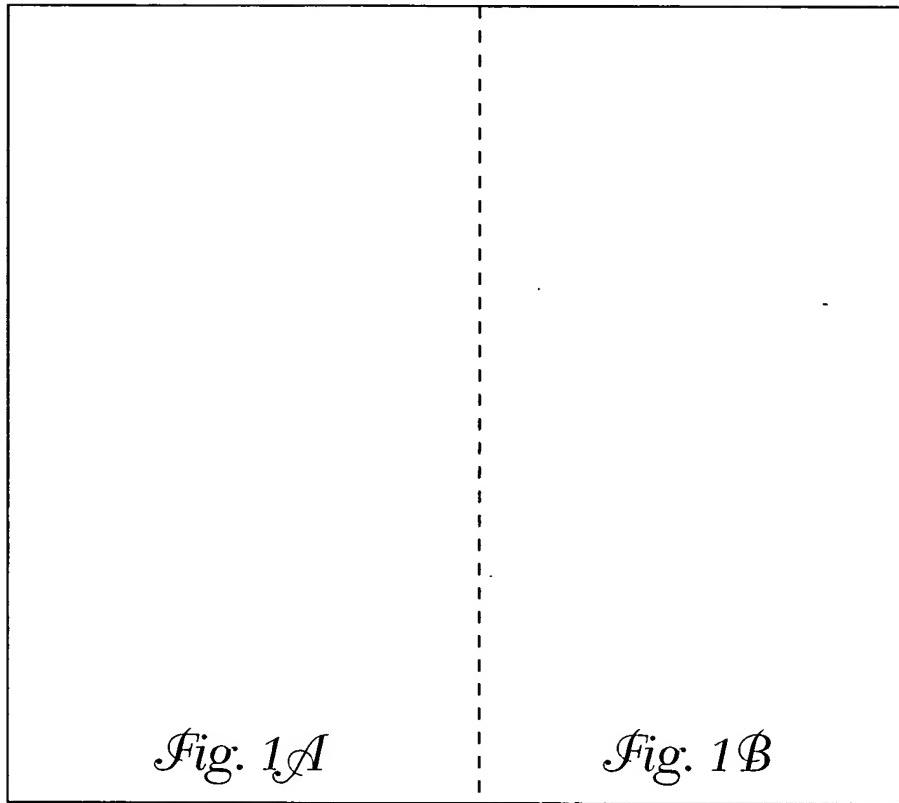


Fig. 1

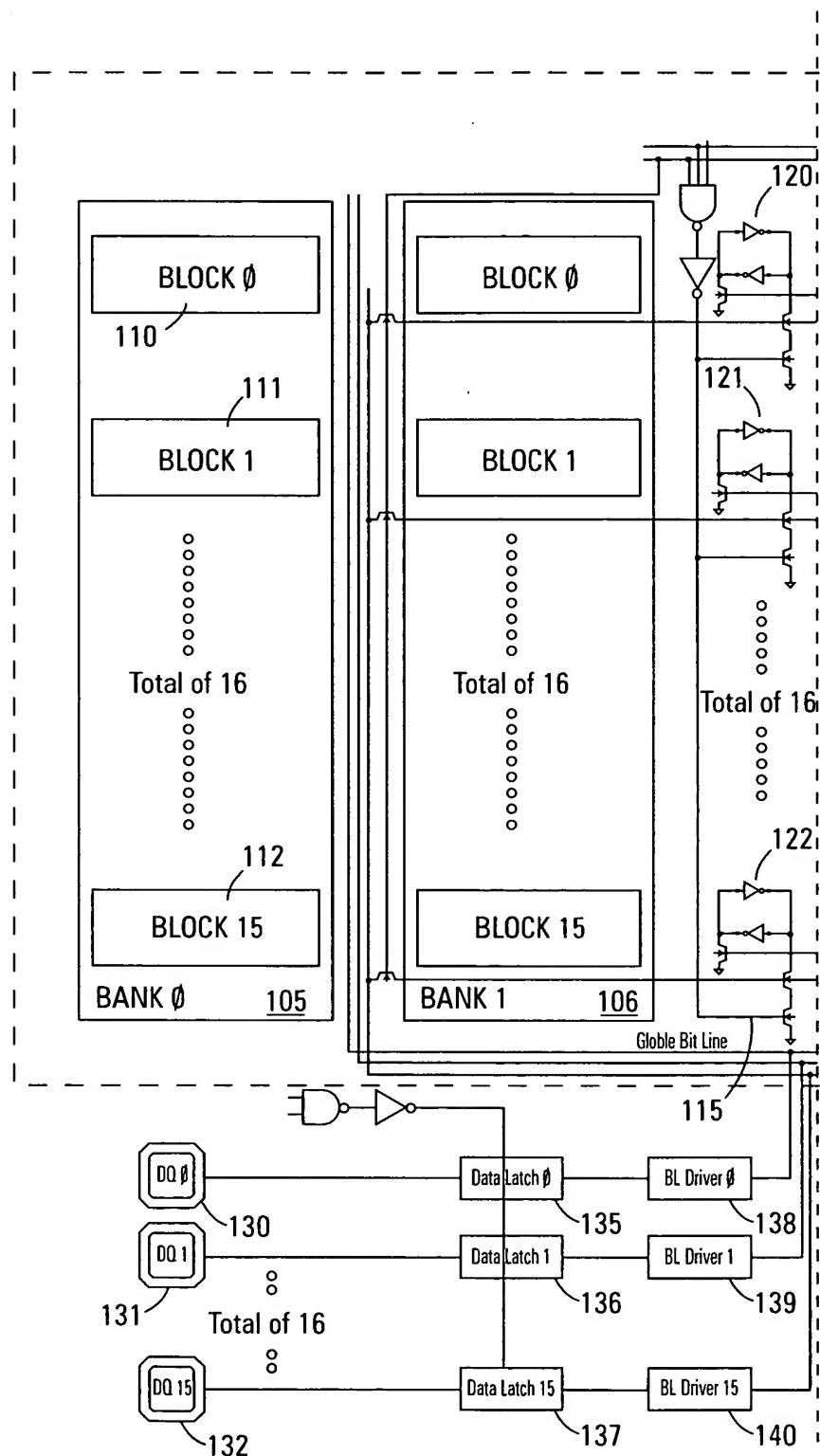


Fig. 1A



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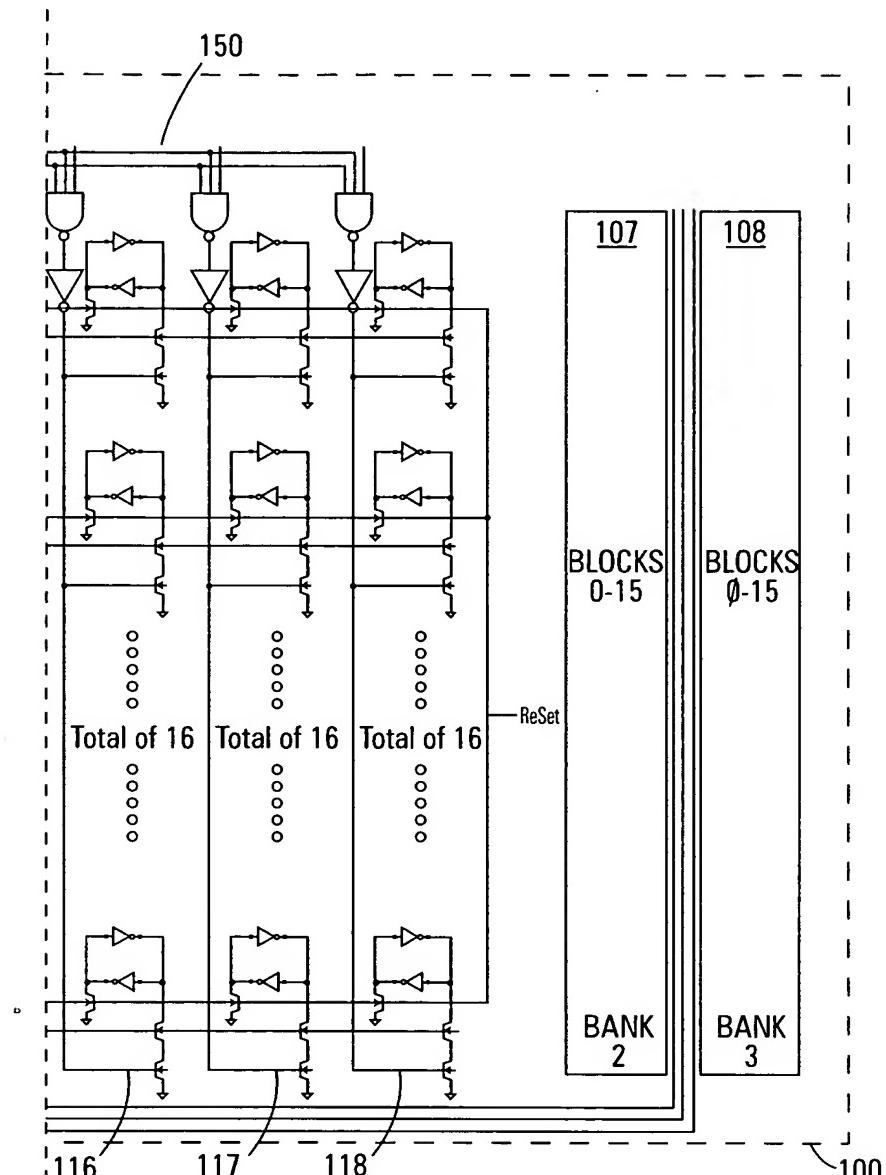


Fig. 1B

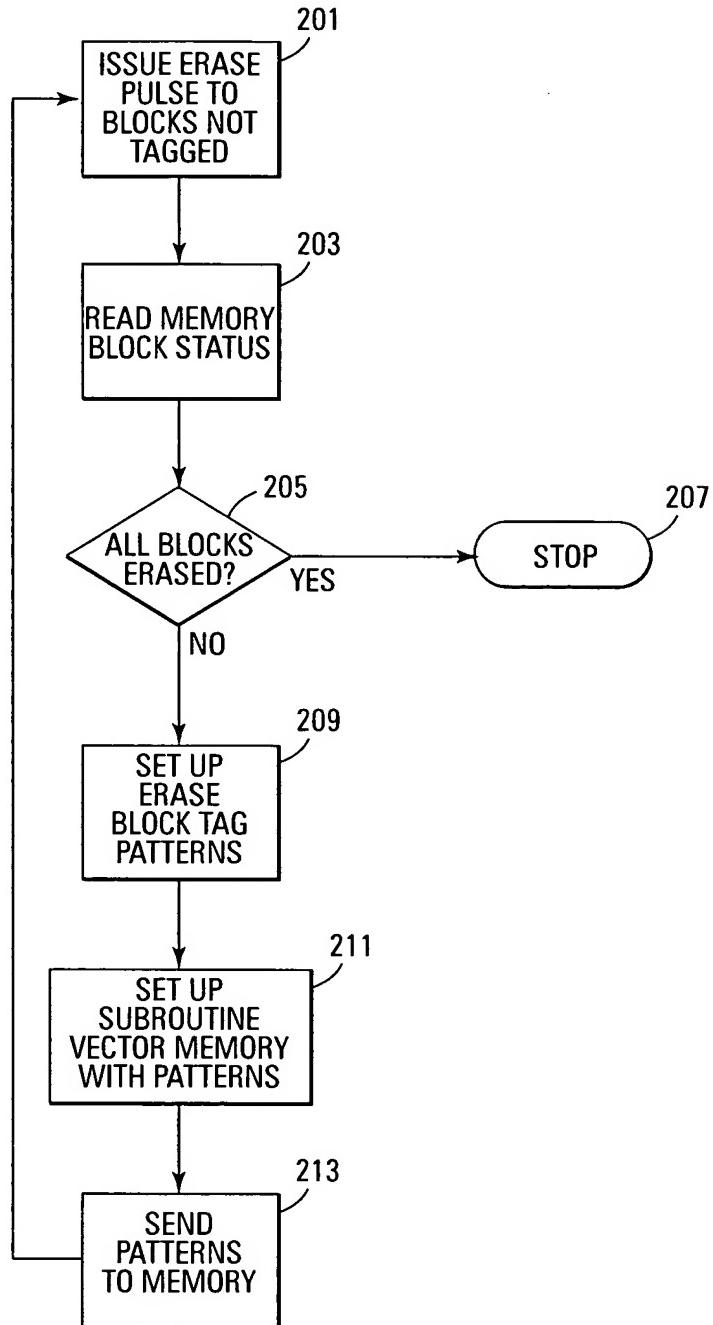


Fig. 2



Sector Address Vector	DQ Vector			
	DUT \emptyset	DUT1	DUT2	DUT3
Sector Addr 0 (Blocks 0-3)	0101	0100	1101	0110
Sector Addr 1 (Blocks 4-7)	0011	1010	0011	1110
Sector Addr 2 (Blocks 8-11)	0001	0000	1001	1000
Sector Addr 3 (Blocks 12-15)	1101	0010	0101	0111

Fig. 3

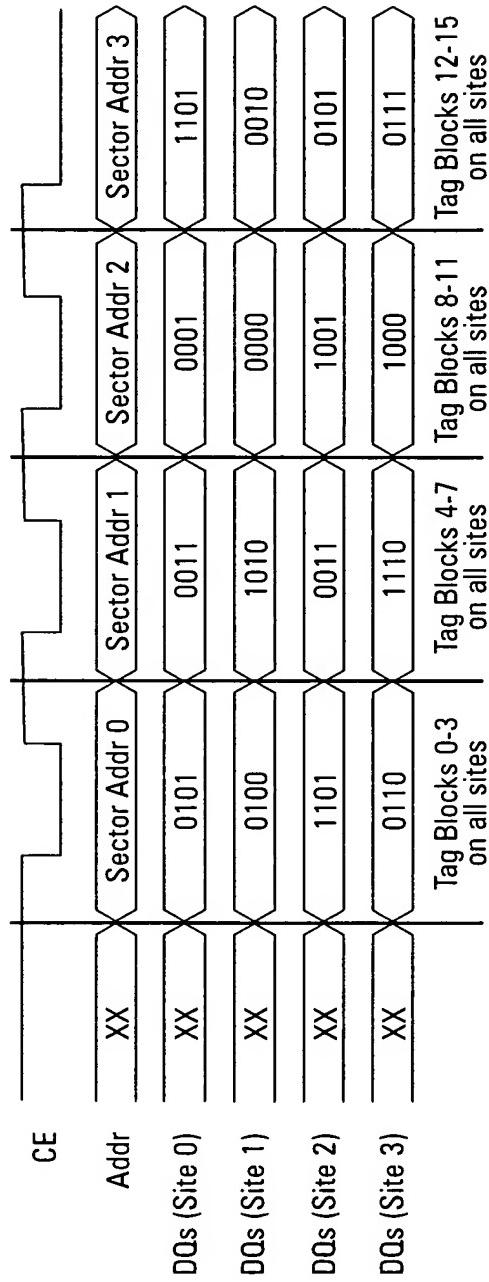


Fig. 4

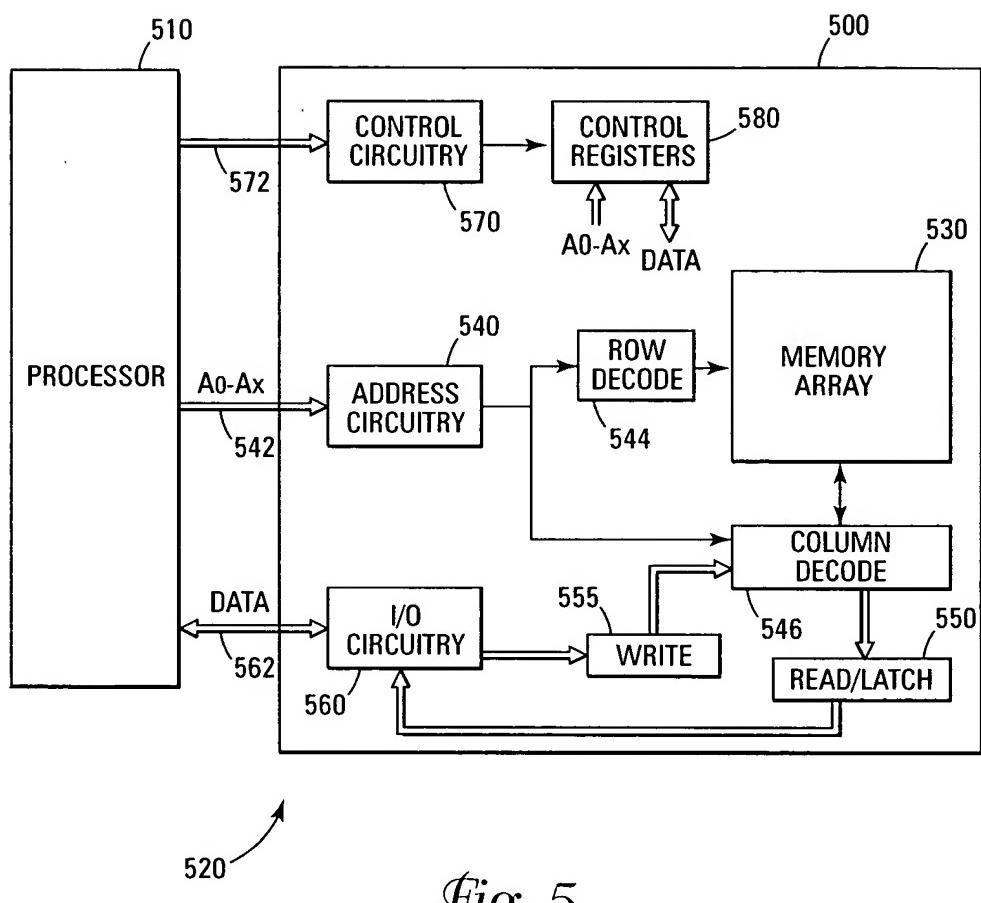


Fig. 5